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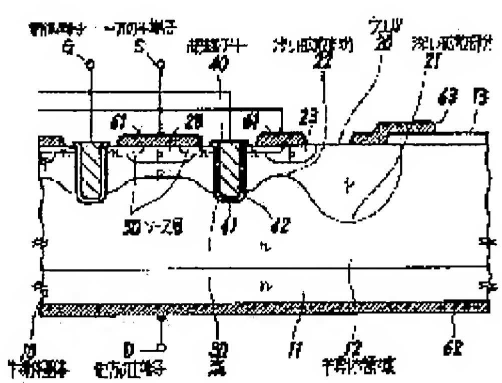
(71)Applicant : FUJI ELECTRIC CO LTD
(72)Inventor : SHIMABUKURO HIROSHI

(54) INSULATED GATE CONTROL SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To improve the with stand voltage and decrease the ON voltage of an insulated gate control semiconductor such as a field effect transistor provided with a buried type insulated gate and an insulated gate bipolar transistor.
CONSTITUTION: From a specified region of the surface of an N-type semiconductor 12 on the surface side of a semiconductor substrate 10, a P-type well 20 is formed in the manner in which a deep diffusion part 21 is formed in the peripheral part and a shallow diffusion part 22 is formed in a part of the inside. A trench 30 is dug from the surface in the vicinity of the shallow diffusion part 22 of the well 20 so as to reach the semiconductor region 12 of the lower side, and an insulating gate is buried in the trench. An N-type source layer 50 is shallowly diffused in the surface of the well 20 which is in contact with the trench 30. One main terminal S is led out from the well 20 and the source layer 50. The other main terminal D is led out from the back side of the substrate 10. A control terminal G is led out from the insulated gate 40. Hence an insulated gate control semiconductor device is obtained.



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CLAIMS

[Claim(s)]
[Claim 1]A well of electric conduction type of another side diffused so that an edge part might form a diffusion portion deeper than an inner part from a prescribed range of the surface of a semiconductor region of one electric conduction type by the side of the surface of a semiconductor base substance, A slot dug deep until it arrived at a lower semiconductor region from the surface of a well inside a deep diffusion portion, An insulated-gate controlled semiconductor device which is provided with a conducted-current type source layer and with which while it was spread in contact with a slot from the insulated gate embedded at Mizouchi and the surface of a well derives [one main terminal] the insulated gate to a control terminal for a main terminal of the rear-face side of a semiconductor base substance to another side from a well and a source layer, respectively.
[Claim 2]A well of electric conduction type of another side diffused so that a part might form a shallow diffusion portion from a prescribed range of the surface of a semiconductor region of one electric conduction type by the side of the surface of a semiconductor base substance, A slot dug deep until it arrived at a lower semiconductor region from the surface near a shallow diffusion portion of a well, In contact with a slot, while was spread from the insulated gate embedded at Mizouchi, and the surface of a well, and it has a conducted-current type source layer, An insulated-gate controlled semiconductor device which derives [one main terminal] the insulated gate to a control terminal for a main terminal of the rear-face side of a semiconductor base substance to another side from a well and a source layer, respectively.
[Claim 3]a process characterized by comprising the following of forming a well, and a well -- with a process dug deep until it arrives at a lower semiconductor region in a slot from the surface near an inner shallow diffusion portion. A process of diffusing a source layer of one electric conduction type shallowly is included in a process of embedding the insulated gate at this Mizouchi, and a portion which touches a slot of the surface of a well, And one [a well and a source layer to] main terminal, A main terminal of the rear-face side of a semiconductor base substance to another side, A manufacturing method of an insulated-gate controlled semiconductor device deriving a control terminal from the insulated gate, respectively

A process of diffusing a deep diffusion portion of a well with conducted type of another side of current from an edge part of a prescribed range of the surface of a semiconductor region of one electric conduction type by the side of the surface of a semiconductor base substance.
this well -- a process of carrying out the ion implantation of the impurity of electric conduction type of another side to the surface of a range with a low dose for a shallow diffusion portion of a well.
a well -- a process of carrying out the ion implantation of the impurity of electric conduction type of another side to some surfaces inside an edge part of a range.
A diffusion portion shallow to the inside of a diffusion portion with a deep edge part made to carry out thermal diffusion of these impurities that carried out the ion implantation.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to insulated-gate controlled semiconductor devices, such as a field effect transistor of embedding gate structure, and an insulated gate bipolar transistor, and the manufacturing method of those.
[0002]
[Description of the Prior Art]The above-mentioned insulated-gate controlled semiconductor device can control the turning on and off by the insulated gate of high input impedance, And there is an advantage which a field effect transistor is suitable for high frequency, and especially an insulated gate bipolar transistor fits for high currents, respectively, It is widely used as an individual semiconductor device, and also these days, the case where it is used in the form included in the chip of the integrated circuit device with the related circuit has increased.
[0003]In this insulated-gate controlled semiconductor device, when including in an integrated circuit device, it is advantageous to consider it as the structure which, of course, repeats a detailed unit cell pattern superficially using integrated circuit art also in the case of a discrete device to improve a high frequency characteristic and make current capacity increase, but. Since the improved efficiency by this minute-pattern-izing is also approaching a limit these days, the flush-type insulated gate structure which stores a gate and attains minuteness making in the slot dug deep in the shape of a trench in the semiconductor has come to be adopted. Hereafter, with reference to drawing 6, the structure of the conventional insulated-gate controlled semiconductor device of this embedding gate structure is explained.
[0004]The insulated-gate controlled semiconductor device shown in drawing 6 is a field effect transistor of end-fire array, and the enlarged section of the end including the two flush-type insulated gates is shown in the figure. The semiconductor base substance 10 which is the wafer thru/or chip for semiconductor devices grows up into a thickness of tens of micrometers the epitaxial layer of n form of specific resistance comparatively high as the semiconductor region 12 which should make the fine structure on the semiconductor substrate 11 of n form, The well 20 of p form is first diffused from the surface of the semiconductor region 12 within the limits surrounded by the wrap field oxide 13 in the surface on the right-hand side of a figure, From the key point of the surface of this well 20, the trench-like slot 30 is dug deep so that it may eat into the lower semiconductor region 12, as shown in a figure, The insulated gate 40 which consists of the gate oxide 41 and the gate 42 of polycrystalline silicon is embedded into it, It is spread very shallowly in high impurity concentration so that the contact layer 23 of p form for the wells 20

may be diffused in high impurity concentration between the slots 30, these contact layers 23 and parts may overlap the source layer 50 of n form and the slot 30 may be touched.
[0005]It is referred to as source terminal S which allocates the metaled electrode layer 61 and connects the contact layer 23 of the well 20 of p form, and the source layer 50 of n form with the surface side of the semiconductor base substance 10 too hastily on the surface, The electrode layer 62 which touches the semiconductor substrate 11 of n form is allocated in the rear-face side, and it is referred to as drain terminal D, and the control terminal G is derived from parts other than the section of a graphic display of the insulated gate 40. In the field effect transistor of this structure, if source terminal S twist positive regulation voltage is received in the control terminal G, One [the channel of n form is formed in the portion pinched in the source layer 50 of n form of the well 20 of p form which touches the gate oxide 41 of the side of the slot 30, and the semiconductor region 12 of n form, and / between source terminal S and drain terminal D]. Thus, since can shorten the mutual interval of the insulated gate 40, and minuteness making of the structure can be carried out, and the perimeter of the side of the slot 30 is covered and a channel is formed by embedding the insulated gate 40 in the slot 30, and making a channel form in a lengthwise direction, current capacity can also be made to increase.
[0006]Since a depletion layer mainly spreads in the semiconductor region 12 of the slot 30 bottom at the time of OFF, set up pressure-proofing of this field effect transistor with the thickness given to the semiconductor region 12, but. Since it is easy to produce a dielectric breakdown along the surface of the field oxide 13 bottom of the semiconductor region 12 near the periphery of the well 20, Simultaneously with allocation of the electrode layer 61, what is called the metaled field plate 63 is formed so that near the periphery of the well 20 may be covered on the field oxide 13, the same potential as the well 20 is applied to this, and a dielectric breakdown is prevented. Although drawing 6 is the structure of a field effect transistor, if it uses the semiconductor substrate 11 as p form and the buffer layer of n form is inserted between the semiconductor regions 12, while it has been the structure as a figure where the upper part is the more nearly same than the semiconductor region 12, it can be used as an insulated gate bipolar transistor.
[0007]
[Problem(s) to be Solved by the Invention]Although structure of an insulated-gate controlled semiconductor device can be minute-pattern-ized, and the high frequency characteristic can be improved or the current capacity can be made to increase by making the insulated gate into a flush type as mentioned above, There is an opposite effect which becomes disadvantageous rather in respect of pressure-proofing since it becomes easy to generate avalanche destruction in the semiconductor region of the slot bottom for the insulated gates in an OFF state, Since the breadth of the channel of the current which flows in a semiconductor region from the channel formed in the side of a slot also by an ON state is not so good, there is a problem on which forward voltage thru/or ON state voltage rise easily. It is drawing 7 (a) about the cause of the followings and these problems. Drawing 7 (b) It is referred to, respectively and explains.
[0008]Drawing 7 (a) It is an expanded sectional view of the important section of the insulated-gate controlled semiconductor device of an OFF state, and signs that a depletion layer spreads in the latter from the pn junction between the well 20 of p form and the semiconductor region 12 of n form are shown to the figure by equipotential surface EP. When the line c along the line b and Si surface in a park of the line of slot 30 directly under and the line d near the curvature part of junction compare the interval of this equipotential surface EP, as shown in a figure, The interval of equipotential surface EP is the narrowest in the direction of the line a of the length of the slot

30 bottom where the insulated gate 40 was embedded, and field intensity is dramatically strong in the part [directly under] of the slot 30 of the semiconductor region 12, and it is easy to generate avalanche destruction. The interval of equipotential surface EP of the direction of line c beside the surface part which touches the field oxide 13 of the semiconductor region 12 can be extended with the above-mentioned field plate 63, and field intensity is eased. Thus, the weak point part which avalanche destruction tends to generate is a directly under part of the slot 30 of the semiconductor region 12, the resisting pressure fall by this weak point should be eased a little, if the slot 30 reduces the depth which projects from the bottom of the well 20, but. actual -- the slot 30 -- from the bottom -- only -- also coming out -- if it projects -- rapid -- element pressure-proofing -- about -- it was checked that a decrease amount becomes still larger as the fall of 150V was seen and the depth of the posterior canal 30 was increased.
[0009]Drawing 7 (b) It is an expanded sectional view of the same important section as the top in an ON state, and channel CP of the electron current which flows in the semiconductor region 12 from the channel Ch formed in the side of the slot 30 is shown in the figure. When current flows into the semiconductor region 12 from the channel Ch of a lengthwise direction, It is known that the depletion region DZ where an electric charge hardly exists by what is called a J-FET effect will spread along the pn junction surface between the well 20 and the semiconductor region 12 from a flowing point of current like a graphic display, Thereby, with the figure in the semiconductor region 12 of current channel CP, since the spreading angle shown by theta is restricted, the current density in this narrow angle theta becomes high, and is considered that the ON state voltage which is a voltage drop in this channel CP increases. Even if it reduced the depth in which there is a limit also in this means although there is room which can improve the increase in ON state voltage by shortening the mutual interval of the slot 30, and the slot 30 projects from the bottom of the well 20 according to the result of the experiment, it turned out that a big improvement effect cannot be expected.
[0010]So to speak, it is an opposite effect, and when [which occurs when each of falls of the above pressure-proofing and increases in ON state voltage aims at improvement in a high frequency characteristic, and the increase in current capacity by adoption of the flush-type insulated gate] improving the performance of an insulated-gate controlled semiconductor device further from the former, the actual condition had become the greatest narrow path. In view of this actual condition, an object of this invention is to decrease respectively the grade which the grade or ON state voltage to which pressure-proofing of an insulated-gate controlled semiconductor device falls also when the insulated gate of a flush type is adopted increases as much as possible.
[0011]
[Means for Solving the Problem]The purpose of preventing the resisting pressure fall according to the insulated-gate controlled semiconductor device of this invention, A well of electric conduction type of another side diffused so that an edge part might form a diffusion portion deeper than an inner part from a prescribed range of the surface of a semiconductor region of one electric conduction type by the side of the surface of a semiconductor base substance, In contact with a slot, while was spread from a slot dug deep until it arrived at a lower semiconductor region from the surface of a well inside this deep diffusion portion, the insulated gate embedded at Mizouchi, and the surface of a well, and after providing a conducted-current type source layer, One [a well and a source layer to] main terminal is attained by deriving a control terminal from the insulated gate, respectively in a main terminal of another side from the rear-face side of a semiconductor base substance. A deep diffusion portion of a well is better than diffusing depth of other portions to make it spread deeply not less than at least 50%. The depth in which a slot

projects caudad from the bottom of a well is more desirable than 3 micrometers or less of little [as much as possible] **. It is advantageous when using 0.5-2 micrometers raises pressure-proofing.

[0012]According to the insulated-gate controlled semiconductor device of this invention, the purpose of preventing an increase in the above-mentioned ON state voltage. A well of electric conduction type of another side diffused so that a part might form a shallow diffusion portion from a prescribed range of the surface of a semiconductor region of one electric conduction type, In contact with a slot, while was spread from a slot dug deep until it arrived at a lower semiconductor region from the surface of a well near a shallow diffusion portion, the insulated gate embedded at Mizouchi, and the surface of a well, and after providing a conducted-current type source layer, One [a well and a source layer to] main terminal is similarly attained by deriving a control terminal from the insulated gate, respectively in a main terminal of another side from the rear-face side of a semiconductor base substance. Diffusing depth of a portion into which a shallow diffusion portion of a well digs a slot deep It is good to make 0.5 micrometers or more shallowly for it to be desirable and shallow 1 micrometers or more. The depth in which a slot projects caudad from the bottom of a well also in this case is advantageous when using little ** suppresses an increase in ON state voltage.

[0013]Composition which uses an edge part of the above-mentioned well as a deep diffusion portion, and composition which uses a part of well as a shallow diffusion portion, By combining mutually and carrying out, the purpose of preventing a pressure-proof fall and an increase in ON state voltage can be attained simultaneously, and especially any composition is suitable for an insulated-gate controlled semiconductor device of end-fire array structure. In order to derive one main terminal from a well, it is good to make a contact layer diffused as usual in the same conducted-current type high impurity concentration as a surface portion of a well of this derivation part.

[0014]In a manufacturing method of an insulated-gate controlled semiconductor device by this invention using a well provided with an above-mentioned deep diffusion portion and a shallow diffusion portion. A deep diffusion portion is first diffused with conducted type of another side of current to an edge part of a range which should make a well of the surface of a semiconductor region of one electric conduction type, While carrying out the ion implantation of the impurity of electric conduction type of another side with a low dose for a diffusion portion shallow on the surface of a range for wells. A well which carries out thermal diffusion of these impurities, and is provided with a shallow diffusion portion inside a deep diffusion portion of an edge part after carrying out the ion implantation of the impurity of electric conduction type of another side to some surfaces inside the edge part is formed, Next, it digs deep until it arrives at a lower semiconductor region in a slot from the surface near a shallow diffusion portion of a well, and the insulated gate is embedded into it, and a source layer of one electric conduction type is shallowly diffused into a portion which touches a slot of the surface of a well further. When providing the above-mentioned contact layer in a surface part of a well, it is advantageous on a process to carry out thermal diffusion of the impurity of electric conduction type of the another side simultaneously with an impurity of one electric conduction type of a source layer.

[0015]

[Function]In this invention, unevenness is provided in the bottom of a well, or a pn junction surface with a semiconductor region.

Therefore, the point which can control the potential distribution at the time of the OFF in a semiconductor region and the current distribution at the time of one is noted, When the insulated

gate is made into a flush type, it succeeds in solution of the problem from the former which the opposite effect which pressure-proofing of an insulated-gate controlled semiconductor device falls as mentioned above, or ON state voltage increases generates.

[0016]Namely, by forming in the edge part of a well the deep diffusion portion said to the composition of the preceding clause, So to speak, the equipotential surface in the semiconductor region of the insulated-gate bottom is caudad depressed from the circumference, it can be made easy to spread in a depletion layer at the time of OFF, this eases the field intensity in the semiconductor region directly under the insulated gate, and pressure-proofing of an insulated-gate controlled semiconductor device is raised conventionally. By forming the shallow diffusion portion said to the composition of the preceding clause, and establishing the slot for the insulated gates in the portion of the well of the neighborhood, the bottom of the well corresponding to a shallow diffusion portion for the depletion region generated by the above-mentioned J-FET effect from the channel of the side of a slot along with the current which flows into a semiconductor region at the time of one -- it being able to dedicate mostly into a hollow so to speak, and, This expands the spreading angle of the current channel in a semiconductor region conventionally, the current density in a channel is reduced, and the ON state voltage of the insulated-gate controlled semiconductor device which is the voltage drop is decreased.
[0017]The manufacturing method of the insulated-gate controlled semiconductor device of this invention is a thing suitable for a make lump of the well possessing an above-mentioned deep diffusion portion and shallow diffusion portion, After diffusing first a diffusion portion deep to the edge part of the range which should make a well in a prescribed depth, the shallow impurity for diffusion portions on the surface of this range with a low dose. After carrying out the ion implantation of the impurity with a predetermined dose to a part of surface inside an edge part, respectively, by carrying out thermal diffusion of them, the deep diffusion portion of a well, a shallow diffusion portion, and the portion for the insulated gates are correctly made in the desired depth from a small routing counter, and it is loaded with them with it, respectively.
[0018]
[Example]Hereafter, the example of this invention is described, referring to a figure. The partial expanded sectional view of the insulated-gate controlled semiconductor device according [drawing 1] to this invention, the sectional view in which drawing 2 expands distribution of the equipotential surface at the time of the OFF, and distribution of the current channel at the time of one, and shows the important section of drawing 1, The diagram in which drawing 3 shows the resisting pressure characteristic, the diagram in which drawing 4 shows the ON-state-voltage characteristic, and drawing 5 are the important section expanded sectional views of the wafer in which the manufacturing method of this invention corresponding to the insulated-gate controlled semiconductor device of drawing 1 is shown in the state for every main processes. Although a well shall be provided with a deep diffusion portion and a shallow diffusion portion in these examples, providing only one side of these in a well can also carry out this invention. Although an insulated-gate controlled semiconductor device is used as a field effect transistor, this invention is applicable also to semiconductor devices, such as a thyristor which are provided with an insulated gate bipolar transistor or the insulated gate, and has similar structure.
[0019]Since the same numerals whose insulated-gate controlled semiconductor device of this invention is the same point as the conventional example of drawing 6 are given to drawing 1 and it is shown in it, below, a mainly different point is explained. The point that the well 20 of p form which differing from structure conventionally made from the surface of the semiconductor

region 12 of n form of the semiconductor base substance 10 equips the edge part with the deep diffusion portion 21, It is a point provided with the shallow diffusion portion 22 near the insulated gate 40 embedded in the slot 30 of the inside, Form the contact layer 23 of p form the source layer 50 of type, and for the n wells 20 which touches the slot 30, and via the electrode layer 61 from the well 20 and the source layer 50. All the points that draw the main terminal D of another side which the main terminal S is drawn and is a drain terminal via the rear-face side of the semiconductor base substance 10 to the electrode layer 62 while it is a source terminal, and derive the control terminal G from the insulated gate 40 are the same as the conventional example of drawing 6. The point that the field plate 63 placed by the well 20 and same electric potential on the field oxide 13 is allocated is also the same.

[0020]Next, the effect which the deep diffusion portion 21 of the well 20 which is the feature of this invention, and the shallow diffusion portion 22 have is explained with reference to drawing 2 corresponding to conventional drawing 7. Drawing 2 (a) Equipotential surface EP shows signs that a depletion layer spreads in the semiconductor region 12 in the state of OFF, Drawing 7 (a) On the whole, a figure turns caudad by the deep diffusion portion 21 of the edge part of the well 20 by inside within the limits which is that left-hand side by a diagram, equipotential surface EP is depressed so that it may turn out that it compares, and a depletion layer spreads easily in the semiconductor region [directly under] 12 of the slot 30 which was the conventional weak point part for this reason. When the impurity concentration of the semiconductor region 12 is 10^{14} - 10^{16} atom / cm^3 Although avalanche destruction occurs in the field intensity of 2.5 - $4x10^{5}$V/cm, In this invention, this field intensity [directly under] of the slot 30 can be eased by the deep diffusion portion 21, and pressure-proofing can be raised. Even when the slot 30 is formed near the shallow diffusion portion 22 like this example, the breadth of the depletion layer in the semiconductor region 12 seldom receives that influence.

[0021]Drawing 2 (b) This example that flowed into the semiconductor region 12 from the channel Ch of the side of the slot 30 in the state of one shows channel CP of electron current. It is drawing 7 (b) about this. Into the hollow of the bottom of the well 20 corresponding to the diffusion portion 22 with the shallow depletion region DZ generated by the above-mentioned J-FET effect since the slot 30 is formed near the shallow diffusion portion 22 so that it may turn out that it compares, as shown in a figure, it is settled mostly, Therefore, spreading angle theta of current channel CP in the semiconductor region 12 is expanded conventionally. Thereby, in this invention, the current density in channel CP can be reduced, the voltage drop can be decreased, and the ON state voltage of an insulated-gate controlled semiconductor device can be decreased. As easily shown in a figure, even when the deep diffusion portion 21 is formed, distribution of current channel CP at the time of this one hardly receives that influence.

[0022]Subsequently, the result of the experiment of an insulated-gate controlled semiconductor device with the structure shown in drawing 1 with reference to drawing 3 and drawing 4 respectively relevant to pressure-proofing and ON state voltage is introduced. Drawing 3 shows the characteristic which the resisting pressure BV or the avalanche break down voltage of a vertical axis to depth d of the slot 30 on the horizontal axis has, and is a case where the characteristic A is this invention, and the characteristic B is a case of the conventional structure of drawing 6 as the comparative example. By this experiment, it is the diffusing depth of the well 20 at structure conventionally corresponding to the characteristic B. As opposed to having been referred to as 4.5 micrometers, Diffusing depth of the diffusion portion 21 deep [in the well 20] with the structure shown in drawing 1 of this invention corresponding to the characteristic A 2 micrometers and the slot 30 of those dig deep the diffusing depth of 4.5 micrometers and the

shallow diffusion portion 22, and it is the diffusing depth of a portion. It could be 2.5 micrometers, respectively. Thickness is [the specific resistance of the semiconductor region 12] 42-ohmcm in 50 micrometers.
[0023]Conventionally, in the characteristic B of structure, while it is smaller than the diffusing depth d1 of the well 20, the resisting pressure BV has depth d of the slot 30 as constant as 700V, but if it exceeds even when depth d of the slot 30 is very slight in the depth d1 of the well 20, the resisting pressure BV will fall to less than 550V quickly. This is conventionally considered for an electric field to concentrate on the semiconductor region [directly under] 12 of the slot 30 with structure. On the other hand, if depth d of the slot 30 exceeds the depth d2 of the well 20 of the portion in the characteristic A in the case of this invention, the resisting pressure BV will fall from the 700V till then, but the degree of a fall becomes less than before all the time, Those with about 650v are obtained for depth d, and, as for the resisting pressure BV, at least 6 micrometers of pressure-proofing of an about [600V] are obtained for depth d at 4 micrometers. This is considered because a depletion layer spreads easily in the semiconductor region [directly under] 12 of the slot 30 by the deep diffusion portion 21 of the edge part of the well 20 and field intensity is eased.
[0024]Drawing 4 shows the dependence characteristic to array-pitch p of the slot 30 or the insulated gate 40 shown on the horizontal axis of ON state voltage FV of the vertical axis at the time of making the well 20 into the same structure as drawing 3. The case where the characteristic B was structure conventionally like a front, it was a case of the structure of drawing 1 by this invention, and the characteristics A1 and A2 set the depth of the slot 30 to 6 micrometers with structure conventionally, and set the depth of the slot 30 to 3 micrometers by 4 micrometers and the characteristic A2 with the characteristic A1 with this invention structure. If array-pitch p of the slot 30 is narrowed to fixed current rating, generally ON state voltage FV will be reduced like a graphic display, but conventionally, in the characteristic B of structure, if array-pitch p is further narrowed from 15-20 micrometers, ON state voltage FV will rise conversely. This is drawing 7 (b), when array-pitch p is narrowed too much. It thinks because the influence of the depletion region DZ becomes strong and spreading angle theta of current channel CP becomes small. On the other hand, the characteristic A1 in the case of this invention and A2 have ON state voltage FV lower than before, and the opposite effect by reduction of array-pitch p hardly shows up, either. This is drawing 2 (b). It thinks for the shallow diffusion portion 22 to shut up the depletion region DZ. In the direction of the characteristic A2 when the slot 30 is shallow, ON state voltage FV becomes low a little, and this is considered because the J-FET effect of the above-mentioned [the one where the projection depth from the bottom of the well 20 of the slot 30 is smaller] becomes minor.
[0025]The depth in which the slot 30 projects from the bottom of the well 20 in the insulated-gate controlled semiconductor device of this invention is more desirable than about 3 micrometers or less so that the characteristic of drawing 3 explained above and drawing 4 may also show. It is advantageous to the improvement in the resisting pressure BV, and reduction of ON state voltage FV to be referred to as 0.5-2 micrometers. Shallow diffusion portion 22 with the diffusion portion 21 deep not less than 50% deeper than the depth of a portion in which the slot 30 of the well 20 digs deep It is advantageous to be spread, respectively so that 0.5 micrometers or more may become it is desirable and shallow 1 micrometers or more shallowly.
[0026]With reference to drawing 5, the manufacturing method of the insulated-gate controlled semiconductor device of this invention corresponding to the structure of drawing 1 is explained to the last. Although a figure is a sectional view of the part corresponding to drawing 1, the

semiconductor region 12 of n form is shown as the semiconductor base substance 10 thru/or a wafer. That whose specific resistance thickness is a 40-ohmcm grade in 50 micrometers is used for this semiconductor region 12 thru/or epitaxial layer. The first drawing 5 (a) It is a diffusion process of the deep diffusion portion 21 for the wells 20. The field oxide 13 on the right-hand side of a figure is a range from which the portion of the left-hand side which was formed of photo etching and surrounded by this from the oxide film of about 1 micrometer of thickness which oxidized the semiconductor region 12 thermally makes the well 20. Drawing 5 (a) After carrying out the ion implantation of the boron to the edge part of this range as p type impurities at a process with the accelerating voltage of for example, 50keV, and the dose about a $4x10^{13}$ atom / cm^2, by the thermal diffusion of 2 to 3 hours under an about 1150 ** elevated temperature. a well -- the deep diffusion portion 21 of ** is made in the predetermined depth. On the occasion of this thermal diffusion, the surface of the semiconductor region 12 is covered with the oxide film 14 of 0.15 - 0.3 mum.

[0027]following drawing 5 (b) a well -- it being an introductory process of the shallow impurity 22a of p form for diffusion partial 22 of **, and, An ion implantation is carried out with the low dose which is a little less than a $4x10^{13}$ atom / cm^2 grade thru/or it through the oxide film 14 to the other whole surface of the semiconductor region 12 under the accelerating voltage of 35 corresponding boron to the thickness - 45keV by using the field oxide 13 as a mask. Continuing drawing 5 (c) Although it is the introductory process of the p type impurities 20a for portions of forming the slot 30 on the well, before that, the low-temperature-oxidation film 15 is formed to 1 micrometer of thickness with a CVD method etc., and the opening of the window is carried out by photo etching. Deviation appears in the depth of the deep diffusion portion 21, and this low-temperature-oxidation film 15 twists, and is needed. Membranes are formed at the low temperature of 400 - 450 **. The ion implantation of the boron as the impurity 20a is carried out by using the low-temperature-oxidation film 15 as a mask with the dose of the $2x10^{3}$ atom / cm^2 under the accelerating voltage of 80 keV.

[0028]Drawing 5 (d) It is a thermal diffusion process which makes the well 20, for example, is considered as the well 20 which carries out simultaneous thermal diffusion of the above-mentioned introductory impurities 22a and 20a by heat treatment of 1 to 2 hours under a 1150 ** elevated temperature, and is provided with the deep diffusion portion 21 and the shallow diffusion portion 22. The deep diffusion portion 21 of the depth of each part of the well 20 is by this. In 4.5 micrometers and the shallow diffusion portion 22, 2 micrometers and other portions. It is set to 2.5 micrometers. As mentioned above, after making the deep diffusion portion 21 from this invention method first, by introducing and carrying out simultaneous thermal diffusion of the impurity in 2 steps, the depth of each portion of the well 20 is correctly controllable by it with a small routing counter.

[0029]Drawing 5 (e) The slot 30 digs deep and it is a process, drawing 1 (c) the dry etching method which uses the formed low-temperature-oxidation film 15 as a mask -- by the reactive-ion-etching method desirably. as [arrive at / penetrate the well 20 and / in the slot 30 of the shape of a trench of 1-2micro width, / the semiconductor region 12 of the bottom] -- for example, after digging deep in depth of 3-4 micrometers, the low-temperature-oxidation film 15 is removed using etching reagents, such as a fluoric acid system, and it changes into the state of a figure where it left only the field oxide 13. Following drawing 5 (f) After being a disposing process of the insulated gate 40 and attaching the very thin gate oxide 41 by complete oxidation first, It changes into the state of a graphic display where the insulated gate 40 was embedded in the slot 30, by growing up the polycrystalline silicon for gate 42 into the whole surface with a

CVD method, as a dashed dotted line shows by a diagram, and performing photo etching. The actual superficial pattern of the slot 30 and the insulated gate 40 is good to consider it as the shape of a ctenidium connected mutually in parts other than the section of a graphic display.

[0030]Drawing 5 (g) Although it is a diffusion process of the source layer 50, as [touch / for them / since the contact layer 23 of p form is formed in the well 20 / in this example, / in boron / the slot 30] -- and to it, after carrying out the ion implantation of the arsenic with high impurity concentration to the n source layers 50 of type, respectively so that the slot 30 may be touched, The source layer 50 of shallow n form and the contact layer 23 of n form deeper than it are made by simultaneous thermal diffusion. The last drawing 5 (h) Are a disposing process of an electrode layer, and with the electrode layer 61 of usual aluminum, short-circuit the surface of the contact layer 23 and the source layer 50, and it is considered as one main terminal S of drawing 1, And the field plate 63 connected with the well 20 from the film of the same aluminum is formed on the field oxide 13. The control terminal G of the insulated gate 40 of drawing 1 is drawn from the connecting part of the ctenidium-like pattern, and the terminal D of another side is drawn from the rear-face side of the semiconductor base substance 10.

[0031]Each portion of the well 20 which has unevenness in the bottom with the above manufacturing method can be made from exact diffusing depth, and an insulated-gate controlled semiconductor device can be stably given with the sufficient reproducibility of pressure-proofing of 600V, and the ON state voltage can also be reduced. The array pitch of the slot 30 to about 10 micrometers or by reducing to less than it and carrying out minuteness making of the pattern, By a field effect transistor, a high frequency characteristic is improved conventionally, with an insulated gate bipolar transistor, hundreds of insulated gates 40 can be arranged to the chip area of several millimeter angle, and the current capacity of the number 10A can be given. The insulated-gate controlled semiconductor device of this invention can give and carry out high-speed operation of a number - the control voltage of 15V to a control terminal.

[0032]Although the deep diffusion portion 21 of the well 20 was formed in the edge part in the example described above, the deep diffusion portion 21 can be formed also inside the well 20 if needed, and the resisting pressure Kougami's effect can be heightened further. In this case, it becomes the structure which put the slot 30 and the insulated gate 40 in the deep diffusion portion 21, and an insulated-gate controlled semiconductor device serves as this structure that composite-ized unit structures so to speak. An area required to make the diffusion portion 21 deep to the inside of the well 20 may be comparable as the above-mentioned array-pitch p of the slot 30 so that an example may show. Thus, without being limited to an example, this invention is unnecessary and can be carried out in various modes according to a case.

[0033]

[Effect of the Invention]As explained above in the insulated-gate controlled semiconductor device of this invention. A well so that a diffusion portion deeper than an inner part may be formed in an edge part from the surface of a semiconductor region, Or the following effect can be mentioned by being spread so that a shallow diffusion portion may be formed in part, digging deep so that the semiconductor region of the bottom may be arrived at in a slot from the surface of a well, embedding the insulated gate into it, and having composition diffused so that a slot may be touched in a source layer from the surface of a well.

[0034](a) By forming a deep diffusion portion in the edge part of a well, digging a slot deep to an inner part shallower than it, and embedding the insulated gate at it, At the time of OFF, in the semiconductor region under a slot, it can be made easy to spread in a depletion layer, the field intensity [directly under] of a slot can be eased, and pressure-proofing of an insulated-gate

controlled semiconductor device can be raised.
(b) By allocating the insulated gate which formed the shallow diffusion portion in the well and was embedded near the in the slot, Confine in the hollow of the bottom of the well corresponding to a shallow diffusion portion the depletion region generated near the point current flows into a semiconductor region from the channel of the side of a slot at the time of one, and the angle of divergence of the current channel in a semiconductor region is made to increase, The current density in a channel is decreased and the ON state voltage of an insulated-gate controlled semiconductor device can be reduced.
[0035](c) Since the pressure-proof improved effect which the above deep diffusion portions have, and the reduction effect of the ON state voltage which a shallow diffusion portion has interfere mutually or are not mutually reduced as the example explained, By forming the both sides of a deep diffusion portion and a shallow diffusion portion in a well, improvement in pressure-proofing of an insulated-gate controlled semiconductor device and reduction of ON state voltage can be attained simultaneously.
[0036](d) Since ON state voltage can also be reduced, minute pattern-ization of an insulated-gate controlled semiconductor device can be advanced further, and it can improve the high frequency characteristic, and it not only makes current capacity increase by reducing the pitch which arranges a slot or the insulated gate, but can raise the current characteristic at the time of one.
In the manufacturing method of the insulated-gate controlled semiconductor device by this invention. After diffusing first a diffusion portion deep to the edge part of the range which should make a well in a prescribed depth, the shallow impurity for diffusion portions on the surface of this range with a low dose. By carrying out simultaneous thermal diffusion of them, after carrying out the ion implantation of the impurity with a predetermined dose to a part of surface inside an edge part, respectively, It is a small routing counter about a well provided with a deep diffusion portion, a shallow diffusion portion, and the portion for the insulated gates, and it can make, managing the depth of these each portion correctly to a desired value, respectively.

[Translation done.]

証拠5

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(71)出願人　000005234
富士電機株式会社
神奈川県川崎市川崎区田辺新田１番１号

(72)発明者　島袋　浩
神奈川県川崎市川崎区田辺新田１番１号
富士電機株式会社内

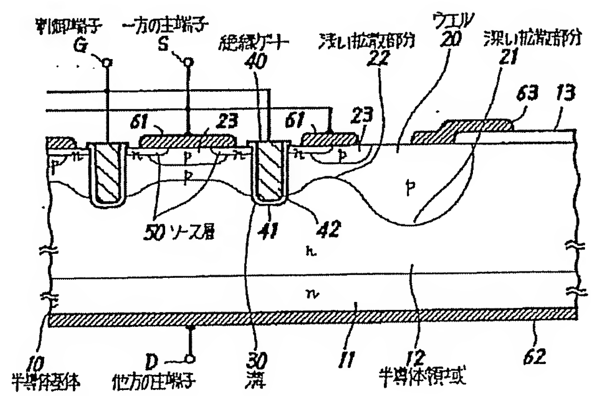
(74)代理人　弁理士　山口　巖

(54)【発明の名称】　絶縁ゲート制御半導体装置とその製造方法

(57)【要約】

【目的】埋め込み形絶縁ゲートを備える電界効果トランジスタや絶縁ゲートバイポーラトランジスタ等の絶縁ゲート制御半導体装置の耐圧を向上しかつそのオン電圧を低減する。

【構成】半導体基体10の表面側のｎ形の半導体領域12の表面の所定範囲からｐ形のウエル20を周縁部に深い拡散部分21，その内側の一部に浅い拡散部分22をそれぞれ形成するように作り込み、このウエル20の浅い拡散部分22の付近の表面から溝30を下側の半導体領域12に達するまで掘り込んでその中に絶縁ゲート40を埋め込み、かつ溝30に接するウエル20の表面にｎ形のソース層50を浅く拡散した上で、ウエル20とソース層50から一方の主端子Ｓを，半導体基体10の裏面側から他方の主端子Ｄを，絶縁ゲート40から制御端子Ｇをそれぞれ導出して絶縁ゲート制御半導体装置とする。



【特許請求の範囲】

【請求項１】半導体基体の表面側の一方の導電形の半導体領域の表面の所定範囲から周縁部が内側部分より深い拡散部分を形成するように拡散された他方の導電形のウエルと、深い拡散部分の内側のウエルの表面から下側の半導体領域に達するまで掘り込まれた溝と、溝内に埋め込まれた絶縁ゲートと、ウエルの表面から溝に接して拡散された一方の導電形のソース層とを備え、ウエルとソース層から一方の主端子を，半導体基体の裏面側から他方の主端子を，絶縁ゲートから制御端子をそれぞれ導出してなる絶縁ゲート制御半導体装置。

【請求項２】半導体基体の表面側の一方の導電形の半導体領域の表面の所定範囲から一部が浅い拡散部分を形成するように拡散された他方の導電形のウエルと、ウエルの浅い拡散部分の付近の表面から下側の半導体領域に達するまで掘り込まれた溝と、溝内に埋め込まれた絶縁ゲートと、ウエルの表面から溝に接して拡散された一方の導電形のソース層とを備え、ウエルおよびソース層から一方の主端子を，半導体基体の裏面側から他方の主端子を，絶縁ゲートから制御端子をそれぞれ導出してなる絶縁ゲート制御半導体装置。

【請求項３】半導体基体の表面側の一方の導電形の半導体領域の表面の所定範囲の周縁部からウエルの深い拡散部分を他方の導電形で拡散する工程と、このウエル範囲の表面にウエルの浅い拡散部分のために他方の導電形の不純物を低いドーズ量でイオン注入する工程と、ウエル範囲の周縁部より内側の一部の表面に他方の導電形の不純物をイオン注入する工程と、これらイオン注入した不純物を熱拡散させて周縁部の深い拡散部分の内側に浅い拡散部分を備えるウエルを形成する工程と、ウエル内の浅い拡散部分の付近の表面から溝を下側の半導体領域に達するまで掘り込む工程と、この溝内に絶縁ゲートを埋め込む工程と、ウエルの表面の溝に接する部分に一方の導電形のソース層を浅く拡散する工程とを含み、かつウエルおよびソース層から一方の主端子を，半導体基体の裏面側から他方の主端子を，絶縁ゲートから制御端子をそれぞれ導出するようにしたことを特徴とする絶縁ゲート制御半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は埋め込みゲート構造の電界効果トランジスタや絶縁ゲートバイポーラトランジスタ等の絶縁ゲート制御半導体装置とその製造方法に関する。

【０００２】

【従来の技術】上述の絶縁ゲート制御半導体装置は高入力インピーダンスの絶縁ゲートによりそのオンオフを制御でき、かつ電界効果トランジスタは高周波用に，絶縁ゲートバイポーラトランジスタは大電流用にそれぞれとくに適する利点があり、個別の半導体素子として広く利用されるほか、最近では関連する回路とともに集積回路装置のチップに組み込んだ形で使用される場合が増加して来た。

【０００３】この絶縁ゲート制御半導体装置では、集積回路装置に組み込む場合はもちろん個別素子の場合でも高周波特性を高め電流容量を増加させるには半導体集積回路技術を利用して微細ユニットセルパターンを平面的に繰り返す構造とするのが有利であるが、最近ではかかる微細パターン化による性能向上も限界に近づきつつあるので、半導体内にトレンチ状に掘り込んだ溝の中にゲートを収納して微細化を図る埋め込み形絶縁ゲート構造が採用されるようになって来た。以下、図６を参照してこの埋め込みゲート構造の従来の絶縁ゲート制御半導体装置の構造を説明する。

【０００４】図６に示す絶縁ゲート制御半導体装置は縦形の電界効果トランジスタであり、図には２個の埋め込み形絶縁ゲートを含むその端部の拡大断面が示されている。半導体装置用のウエハないしチップである半導体基体10はｎ形の半導体基板11の上に微細構造を作り込むべき半導体領域12として比較的高い比抵抗のｎ形のエピタキシャル層を数十μｍの厚みに成長させたものであり、図の右側のその表面を覆うフィールド酸化膜13で取り囲まれた範囲内の半導体領域12の表面からｐ形のウエル20をまず拡散し、このウエル20の表面の要所からトレンチ状の溝30を図のように下側の半導体領域12に食い込むよう掘り込み、その中にゲート酸化膜41と多結晶シリコンのゲート42とからなる絶縁ゲート40を埋め込み、溝30の相互間にウエル20用のｐ形のコンタクト層23を高不純物濃度で拡散し、かつｎ形のソース層50をこのコンタクト層23と一部が重なり合いかつ溝30に接するように高不純物濃度でごく浅く拡散する。

【０００５】さらに、半導体基体10の表面側に金属の電極膜61を配設してｐ形のウエル20のコンタクト層23とｎ形のソース層50を表面で短絡するソース端子Ｓとし、裏面側にはｎ形の半導体基板11に接する電極膜62を配設してドレイン端子Ｄとし、かつ絶縁ゲート40の図示の断面以外の個所から制御端子Ｇを導出する。かかる構造の電界効果トランジスタでは、その制御端子Ｇにソース端子Ｓより正の制御電圧を受けると、溝30の側面のゲート酸化膜41に接するｐ形のウエル20のｎ形のソース層50とｎ形の半導体領域12で挟まれた部分にｎ形のチャネルが形成されてソース端子Ｓとドレイン端子Ｄの間がオンする。このように、絶縁ゲート40を溝30内に埋め込んでチャネルを縦方向に形成させることにより絶縁ゲート40の相互間隔を短縮して構造を微細化することができ、かつ溝30の側面の全周に亘りチャネルが形成されるので電流容量も増加させることができる。

【０００６】なお、オフ時に空乏層が主に溝30の下側の半導体領域12内に広がるので、この電界効果トランジスタの耐圧は半導体領域12にもたせる厚みにより設定する

が、ウエル20の周縁付近の半導体領域12のフィールド酸化膜13の下側の表面に沿って絶縁破壊が生じやすいため、電極膜61の配設と同時に金属のいわゆるフィールドプレート63をフィールド酸化膜13の上にウエル20の周縁付近を覆うように設け、これにウエル20と同じ電位を掛けて絶縁破壊を防止する。また、図６は電界効果トランジスタの構造であるが、半導体基板11をｐ形としかつｎ形のバッファ層を半導体領域12との間に挿入すれば、半導体領域12より上側部分が図と同じ構造のままで絶縁ゲートバイポーラトランジスタとすることができる。

【０００７】

【発明が解決しようとする課題】上述のように絶縁ゲートを埋め込み形とすることにより絶縁ゲート制御半導体装置の構造を微細パターン化してその高周波特性を高めあるいはその電流容量を増加させることができるが、オフ状態で絶縁ゲート用の溝の下側の半導体領域にアバランシェ破壊が発生しやすくなるため耐圧の点でむしろ不利になる逆効果があり、オン状態でも溝の側面に形成されるチャネルから半導体領域内に流入する電流の流路の広がりがあまり良好でないために順方向電圧ないしオン電圧が上昇しやすくなる問題がある。以下、これらの問題点の原因を図７(a) と図７(b) をそれぞれ参照して説明する。

【０００８】図７(a) はオフ状態の絶縁ゲート制御半導体装置の要部の拡大断面図であり、図にはｐ形のウエル20とｎ形の半導体領域12の間のpn接合から空乏層が後者内に広がる様子が等電位面EPで示されている。この等電位面EPの間隔を溝30直下の線の、バルク中の線ｂ、Si表面に沿った線ｃ、接合の曲率部近くの線ｄで比較すると図からわかるように、絶縁ゲート40が埋め込まれた溝30の下側の縦の線ａの方向で等電位面EPの間隔が最も狭くなっており、半導体領域12の溝30の直下の個所で電界強度が非常に強くてアバランシェ破壊が発生しやすい。半導体領域12のフィールド酸化膜13に接する表面部の横の線ｃ方向の等電位面EPの間隔は前述のフィールドプレート63により広げられ、電界強度が緩和されている。このように、アバランシェ破壊が最も発生しやすい弱点部は半導体領域12の溝30の直下部であり、この弱点による耐圧低下は溝30がウエル20の底面から突出する深さを減らせば若干は緩和されるはずであるが、実際には溝30が底面からわずかでも突出すると急激に素子耐圧に約150Vの低下が見られ、その後溝30の深さを増すにつれて低下量はさらに大きくなっていくことが確認された。

【０００９】図７(b) はオン状態における上と同じ要部の拡大断面図であり、図には溝30の側面に形成されたチャネルChから半導体領域12内に流入する電子電流の流路CPが示されている。電流が縦方向のチャネルChから半導体領域12に流入する場合は、いわゆる J-FET効果により電荷がほとんど存在しない空乏領域DZが図示のように電流の流入点からウエル20と半導体領域12の間のpn接合面に沿って広がることが知られており、これにより電流流路CPの半導体領域12内の図ではθで示す広がり角度が制限されるのでこの狭い角度θ内の電流密度が高くなり、この流路CP内の電圧降下であるオン電圧が増加するものと考えられる。実験の結果によればオン電圧の増加を溝30の相互間隔を短縮することにより改善できる余地はあるがこの手段にも限度があり、また溝30がウエル20の底面から突出する深さを減らしても大きな改善効果は望めないことがわかった。

【００１０】以上のような耐圧の低下やオン電圧の増加はいずれも埋め込み形絶縁ゲートの採用により高周波特性の向上や電流容量の増加を図る際に起きるいわば逆効果であり、従来から絶縁ゲート制御半導体装置の性能を一層高める上で最大の隘路になっていたのが実情である。かかる現状に鑑み、本発明は埋め込み形の絶縁ゲートを採用した場合にも絶縁ゲート制御半導体装置の耐圧が低下する程度ないしはオン電圧が増加する程度を各々できるだけ減少させることを目的とするものである。

【００１１】

【課題を解決するための手段】本発明の絶縁ゲート制御半導体装置によればその耐圧低下を防止する目的は、半導体基体の表面側の一方の導電形の半導体領域の表面の所定範囲から周縁部が内側部分より深い拡散部分を形成するよう拡散された他方の導電形のウエルと，この深い拡散部分の内側のウエルの表面から下側の半導体領域に達するまで掘り込まれた溝と，溝内に埋め込まれた絶縁ゲートと，ウエルの表面から溝に接して拡散された一方の導電形のソース層を設けた上で、ウエルとソース層から一方の主端子を，半導体基体の裏面側から他方の主端子を，絶縁ゲートから制御端子をそれぞれ導出することによって達成される。なお、ウエルの深い拡散部分は他の部分の拡散深さよりも少なくとも50%以上深く拡散させるのがよい。また、溝がウエルの底面から下方に突出する深さは極力少ないめの例えば３μｍ以下，より望ましくは 0.5～２μｍにするのが耐圧を高める上で有利である。

【００１２】また、前述のオン電圧の増加を防止する目的は本発明の絶縁ゲート制御半導体装置によれば、一方の導電形の半導体領域の表面の所定範囲から一部が浅い拡散部分を形成するよう拡散された他方の導電形のウエルと，浅い拡散部分の付近のウエルの表面から下側の半導体領域に達するまで掘り込まれた溝と，溝内に埋め込まれた絶縁ゲートと，ウエルの表面から溝に接して拡散された一方の導電形のソース層とを設けた上で、同様にウエルとソース層から一方の主端子を，半導体基体の裏面側から他方の主端子を，絶縁ゲートから制御端子をそれぞれ導出することにより達成される。なお、ウエルの浅い拡散部分は溝を掘り込む部分の拡散深さよりも 0.5μｍ以上浅く，望ましくは１μｍ以上浅くするのがよい。また、この場合も溝がウエルの底面から下方に突出

する深さは少ないめにするのがオン電圧の増加を抑える上で有利である。

【0013】上記のウエルの周縁部を深い拡散部分とする構成と，ウエルの一部を浅い拡散部分とする構成とは、互いに組み合わせて実施することにより耐圧の低下とオン電圧の増加を防止する目的を同時に達成でき、いずれの構成もとくに縦形構造の絶縁ゲート制御半導体装置に適する。また、ウエルから一方の主端子を導出するため従来と同様にこの導出部のウエルの表面部分に同じ導電形の高不純物濃度で拡散されたコンタクト層を作り込むのがよい。

【0014】上述の深い拡散部分および浅い拡散部分を備えるウエルを用いる本発明による絶縁ゲート制御半導体装置の製造方法では、一方の導電形の半導体領域の表面のウエルを作り込むべき範囲の周縁部に対して深い拡散部分を他方の導電形でまず拡散し、ウエル用の範囲の表面に浅い拡散部分のために他方の導電形の不純物を低いドーズ量でイオン注入するとともにその周縁部の内側の一部の表面に他方の導電形の不純物をイオン注入した上でこれら不純物を熱拡散させて周縁部の深い拡散部分の内側に浅い拡散部分を備えるウエルを形成し、次にウエルの浅い拡散部分の付近の表面から溝を下側の半導体領域に達するまで掘り込みかつその中に絶縁ゲートを埋め込み、さらにウエルの表面の溝に接する部分に一方の導電形のソース層を浅く拡散する。なお、ウエルの表面部に前述のコンタクト層を設ける場合は、その他方の導電形の不純物をソース層の一方の導電形の不純物と同時に熱拡散させるのが工程上有利である。

【0015】

【作用】本発明はウエルの底面ないしは半導体領域とのpn接合面に凹凸を設けることにより半導体領域内のオフ時の電位分布やオン時の電流分布を制御できる点に着目して、絶縁ゲートを埋め込み形にした場合に前述のように絶縁ゲート制御半導体装置の耐圧が低下したりオン電圧が増加したりする逆効果が発生する従来からの問題点の解決に成功したものである。

【0016】すなわち、前項の構成にいう深い拡散部分をウエルの周縁部に形成することにより、絶縁ゲートの下側の半導体領域内の等電位面をいわば周囲から下方に押し下げてオフ時に空乏層を広がりやすくすることができ、これにより絶縁ゲートの直下の半導体領域内の電界強度を緩和して、絶縁ゲート制御半導体装置の耐圧を従来よりも向上させるものである。また、前項の構成にいう浅い拡散部分を形成してその付近のウエルの部分に絶縁ゲート用の溝を設けることにより、オン時に溝の側面のチャネルから半導体領域に流入する電流に付随して前述の J-FET効果により発生する空乏領域を浅い拡散部分に対応するウエルの底面のいわば凹所の中にほぼ納めてしまうことができ、これにより半導体領域内の電流流路の広がり角度を従来より拡大して流路内の電流密度を低下させ、その電圧降下である絶縁ゲート制御半導体装置のオン電圧を減少させるものである。

【0017】さらに、本発明の絶縁ゲート制御半導体装置の製造方法は上述の深い拡散部分および浅い拡散部分を具備するウエルの作り込みに適するもので、ウエルを作り込むべき範囲の周縁部に深い拡散部分を所定深さにまず拡散した後、この範囲の表面に浅い拡散部分用の不純物を低いドーズ量で，周縁部の内側の表面の一部に不純物を所定ドーズ量でそれぞれイオン注入した上でそれらを熱拡散させることにより、少ない工程数でウエルの深い拡散部分と浅い拡散部分と絶縁ゲート用の部分をそれぞれ所望の深さに正確に作り込めるようにするものである。

【0018】

【実施例】以下、図を参照しながら本発明の実施例を説明する。図１は本発明による絶縁ゲート制御半導体装置の一部拡大断面図、図２はそのオフ時の等電位面の分布とオン時の電流流路の分布を図１の要部を拡大して示す断面図、図３は耐圧特性を示す線図、図４はオン電圧特性を示す線図、図５は図１の絶縁ゲート制御半導体装置に対応する本発明の製造方法を主な工程ごとの状態で示すウエハの要部拡大断面図である。なお、これら実施例ではウエルが深い拡散部分と浅い拡散部分を備えるものとするが、これらの内の一方だけをウエルに設けることでも本発明を実施できる。また、絶縁ゲート制御半導体装置は電界効果トランジスタとするが本発明は絶縁ゲートバイポーラトランジスタや絶縁ゲートを備えかつ類似構造をもつサイリスタ等の半導体装置にも適用できる。

【0019】図１には本発明の絶縁ゲート制御半導体装置が図６の従来例と同じ要領でかつ同じ符号を付して示されているので、以下では主に異なる点について説明する。従来構造と異なるのは半導体基体10のｎ形の半導体領域12の表面から作り込んだｐ形のウエル20がその周縁部に深い拡散部分21を備える点と、その内側の溝30に埋め込まれた絶縁ゲート40の付近に浅い拡散部分22を備える点であって、溝30に接するｎ形のソース層50とウエル20用のｐ形のコンタクト層23を設け，ウエル20とソース層50から電極膜61を介してソース端子である一方の主端子Ｓを導出し，半導体基体10の裏面側から電極膜62を介しドレイン端子である他方の主端子Ｄを導出し，かつ絶縁ゲート40から制御端子Ｇを導出する点はすべて図６の従来例と同じである。フィールド酸化膜13の上にウエル20と同電位に置かれるフィールドプレート63が配設されている点も同じである。

【0020】次に、本発明の特徴であるウエル20の深い拡散部分21と浅い拡散部分22がもつ効果を従来の図７に対応する図２を参照して説明する。図２(a) はオフの状態で半導体領域12内に空乏層が広がる様子を等電位面EPで示し、図７(a) と比べるとわかるように等電位面EPがウエル20の周縁部の深い拡散部分21により図ではその左

側である内側範囲内で全体的に図の下方に向け押し下げられ、このため従来の弱点部であった溝30の直下の半導体領域12に空乏層が広がりやすくなる。半導体領域12の不純物濃度が10^{14}〜10^{16}原子／cm^3 のとき 2.5〜4 x10^5 V／cmの電界強度でアバランシェ破壊が発生するが、本発明では溝30の直下のこの電界強度を深い拡散部分21により緩和して耐圧を向上させることができる。なお、この例のように浅い拡散部分22の付近に溝30を設けた場合でも半導体領域12内の空乏層の広がりはあまりその影響を受けない。

【００２１】図２(b) はオンの状態で溝30の側面のチャネルChから半導体領域12に流入したこの例では電子電流の流路CPを示す。これを図７(b) と比べるとわかるように、浅い拡散部分22の付近に溝30が設けられるので前述の J-FET効果により発生する空乏領域DZが浅い拡散部分22に対応するウエル20の底面の凹所の中に図のようにほぼ納まってしまい、従って半導体領域12内の電流流路CPの広がり角度θが従来より拡大される。これにより、本発明では流路CP内の電流密度を低下させてその電圧降下を減少させ、絶縁ゲート制御半導体装置のオン電圧を減少させることができる。なお、図から容易にわかるように深い拡散部分21を設けた場合でもこのオン時の電流流路CPの分布はほとんどその影響を受けない。

【００２２】ついで、図３と図４を参照して図１に示した構造をもつ絶縁ゲート制御半導体装置のそれぞれ耐圧とオン電圧に関連する実験の結果を紹介する。図３は横軸の溝30の深さｄに対する縦軸の耐圧BVないしはアバランシェ破壊電圧がもつ特性を示すもので、特性Ａが本発明の場合であり、特性Ｂはその比較例としての図６の従来構造の場合である。この実験では特性Ｂに対応する従来構造ではウエル20の拡散深さを 4.5μｍとしたのに対し、特性Ａに対応する本発明の図１に示す構造ではウエル20内の深い拡散部分21の拡散深さを 4.5μm，浅い拡散部分22の拡散深さを２μm，その溝30の掘り込み部分の拡散深さを 2.5μｍとそれぞれした。なお、半導体領域12は厚みが50μｍで比抵抗が42Ωcmである。

【００２３】従来構造の特性Ｂでは、溝30の深さｄがウエル20の拡散深さd1より小さい間は耐圧BVは700Vと一定であるが、溝30の深さｄがウエル20の深さd1をごく僅かでも越えると耐圧BVは550V以下に急速に低下する。これは従来構造では溝30の直下の半導体領域12に電界が集中するためと考えられる。これに対し、本発明の場合の特性Ａでは溝30の深さｄがその部分のウエル20の深さd2を越えると耐圧BVはそれまでの700Vからは下がるが低下の度合いは従来よりずっと少なくなり、深さｄが４μｍで耐圧BVは約650Vあり、深さｄが６μｍでも600V程度の耐圧が得られる。これは、ウエル20の周縁部の深い拡散部分21により溝30の直下の半導体領域12に空乏層が広がりやすくなって電界強度が緩和されるためと考えられる。

【００２４】図４はウエル20を図３と同じ構造にした場合の縦軸のオン電圧FVの横軸に示す溝30ないしは絶縁ゲート40の配列ピッチｐに対する依存特性を示す。前と同様に特性Ｂが従来構造の場合，特性A1とA2が本発明による図１の構造の場合であり、従来構造では溝30の深さを６μｍとし、本発明構造では溝30の深さを特性A1では４μm，特性A2では３μｍとした。一定の電流定格に対し溝30の配列ピッチｐを狭めるとオン電圧FVは図示のように一般に低減されるが、従来構造の特性Ｂでは配列ピッチｐを15〜20μｍよりさらに狭めるとオン電圧FVは逆に上昇して来る。これは、配列ピッチｐを狭め過ぎると図７(b) の空乏領域DZの影響が強まり電流流路CPの広がり角度θが小さくなるためと考えられる。これに対して、本発明の場合の特性A1やA2はオン電圧FVが従来より低く、かつ配列ピッチｐの縮小による逆効果もほとんど現れない。これは、図２(b) の浅い拡散部分22が空乏領域DZを閉じ込めるためと考えられる。また、溝30が浅い時の特性A2の方がオン電圧FVが若干低くなり、これは溝30のウエル20の底面からの突出深さが小さい方が前述のJ-FET効果が軽微になるためと考えられる。

【００２５】以上説明した図３と図４の特性からもわかるように、本発明の絶縁ゲート制御半導体装置では溝30がウエル20の底面から突出する深さは３μｍ程度以下，より望ましくは 0.5〜２μｍとするのが耐圧BVの向上およびオン電圧FVの低減に有利である。さらに、ウエル20の溝30の掘り込み部分の深さよりも深い拡散部分21は50％以上深く，浅い拡散部分22は 0.5μｍ以上浅く，望ましくは１μｍ以上浅くなるようにそれぞれ拡散するのが有利である。

【００２６】最後に、図５を参照して図１の構造に対応する本発明の絶縁ゲート制御半導体装置の製造方法を説明する。図は図１に対応する個所の断面図であるが、半導体基体10ないしウエハとしてそのｎ形の半導体領域12が示されている。この半導体領域12ないしエピタキシャル層には例えば厚みが50μｍで比抵抗が40Ωcm程度のものが用いられる。最初の図５(a) はウエル20用の深い拡散部分21の拡散工程である。図の右側のフィールド酸化膜13は半導体領域12を熱酸化した１μｍ程度の膜厚の酸化膜からフォトエッチングにより形成され、これにより囲まれた左側の部分がウエル20を作り込む範囲である。図５(a) の工程ではこの範囲の周縁部にｐ形不純物としてボロンを例えば50keV の加速電圧， ４ x10^{13}原子／cm^2 程度のドーズ量でイオン注入した後に1150℃程度の高温下の２〜３時間の熱拡散によりウエル用の深い拡散部分21を所定の深さに作り込む。この熱拡散に際して半導体領域12の表面は0.15〜0.3 μｍの酸化膜14で覆われる。

【００２７】次の図５(b) はウエル用の浅い拡散部分22用のｐ形の不純物22ａの導入工程であり、フィールド酸化膜13をマスクとして半導体領域12のそれ以外の全面に対しボロンを酸化膜14を通してその厚みに応じた35〜45

keVの加速電圧下で４ｘ10^{13}原子／cm^2 程度ないしそれを若干下回る低いドーズ量でイオン注入する。つづく図５(c) はウエルの溝30を設ける部分用のｐ形不純物20ａの導入工程であるが、その前に低温酸化膜15をＣＶＤ法等により例えば１μｍの膜厚に成膜してフォトエッチングによって窓を開口する。この低温酸化膜15は深い拡散部分21の深さに狂いが出ないよう 400～450 ℃の低温で成膜する。不純物20ａとしてのボロンは低温酸化膜15をマスクとして例えば80 keVの加速電圧下の２ｘ10^3 原子／cm^2 のドーズ量でイオン注入する。

【００２８】図５(d) はウエル20を作り込む熱拡散工程であって、例えば1150℃の高温下の１～２時間の熱処理により上述の導入不純物22ａと20ａを同時熱拡散させて深い拡散部分21と浅い拡散部分22を備えるウエル20とする。これによってウエル20の各部の深さは例えば深い拡散部分21が 4.5μｍ，浅い拡散部分22が２μｍ，他の部分が 2.5μｍとなる。以上のように本発明方法では深い拡散部分21をまず作り込んだ上で不純物を２回に分けて導入して同時熱拡散させることにより、少ない工程数でウエル20の各部分の深さを正確に制御することができる。

【００２９】図５(e) は溝30の掘り込み工程であって、図１(c) で形成した低温酸化膜15をマスクとするドライエッチング法，望ましくはリアクティブイオンエッチング法によって１～２μ幅のトレンチ状の溝30をウエル20を貫通してその下側の半導体領域12に達するように，例えば３～４μｍの深さに掘り込んだ後、ふっ酸系等のエッチング液を用いて低温酸化膜15を除去し、フィールド酸化膜13のみを残した図の状態とする。次の図５(f) は絶縁ゲート40の配設工程であり、まず全面酸化によりごく薄いゲート酸化膜41を付けた後、ＣＶＤ法によりゲート42用の多結晶シリコンを図では一点鎖線で示すよう全面に成長させ、かつフォトエッチングを施すことにより溝30内に絶縁ゲート40が埋め込まれた図示の状態とする。なお、溝30と絶縁ゲート40の実際の平面的なパターンは図示の断面以外の個所で相互に連結された櫛歯状とするのがよい。

【００３０】図５(g) はソース層50の拡散工程であるが、この実施例ではウエル20にｐ形のコンタクト層23を設けるのでそれ用にボロンを溝30と接しないよう，かつｎ形のソース層50用に例えば砒素を溝30と接するようにそれぞれ高不純物濃度でイオン注入した上で、同時熱拡散により浅いｎ形のソース層50とそれよりも深いｎ形のコンタクト層23を作り込む。最後の図５(h) は電極膜の配設工程であり、通例のアルミの電極膜61によってコンタクト層23とソース層50の表面を短絡して図１の一方の主端子Ｓとし、かつ同じアルミの膜からウエル20と接続されたフィールドプレート63をフィールド酸化膜13の上に形成する。なお、図１の絶縁ゲート40の制御端子Ｇはその櫛歯状パターンの連結部から導出され、他方の端子Ｄは半導体基体10の裏面側から導出される。

【００３１】以上の製造方法により底面に凹凸をもつウエル20の各部分を正確な拡散深さで作り込んで、絶縁ゲート制御半導体装置に例えば600Vの耐圧の再現性よく安定にもたせ、かつそのオン電圧も低減することができる。また、溝30の配列ピッチを10μｍ程度にないしそれ以下に縮小してパターンを微細化することにより、電界効果トランジスタでは高周波特性を従来より高め、絶縁ゲートバイポーラトランジスタでは数mm角のチップ面積に数百個の絶縁ゲート40を配列して数十Ａの電流容量をもたせることができる。本発明の絶縁ゲート制御半導体装置は制御端子に数～15Ｖの制御電圧を与えて高速動作させることができる。

【００３２】なお、以上述べた実施例ではウエル20の深い拡散部分21をその周縁部に設けるようにしたが、必要に応じてウエル20の内側にも深い拡散部分21を形成してその耐圧向上の効果を一層高めることができる。この場合は深い拡散部分21で溝30や絶縁ゲート40を挟み込んだ構造となり、絶縁ゲート制御半導体装置はこのいわば単位構造を複合化した構造となる。実施例からわかるように、ウエル20の内側に深い拡散部分21を作り込むに必要な面積は溝30の前述の配列ピッチｐと同程度でよい。このように、本発明は実施例に限定されることなく必要ないし場合に応じ種々の態様で実施をすることができる。

【００３３】

【発明の効果】以上説明したとおり本発明の絶縁ゲート制御半導体装置では、ウエルを半導体領域の表面から周縁部に内側部分よりも深い拡散部分を形成するよう，あるいは一部に浅い拡散部分を形成するように拡散し、ウエルの表面から溝をその下側の半導体領域に達するように掘り込んでその中に絶縁ゲートを埋め込み、ウエルの表面からソース層を溝に接するよう拡散する構成とすることにより、次の効果を挙げることができる。

【００３４】(a) ウエルの周縁部に深い拡散部分を形成してそれよりも浅い内側部分に溝を掘り込んで絶縁ゲートを埋め込むことにより、オフ時に溝の下の半導体領域内に空乏層を広がりやすくして溝の直下の電界強度を緩和し、絶縁ゲート制御半導体装置の耐圧を向上させることができる。

(b) ウエルに浅い拡散部分を形成してその付近に溝に埋め込んだ絶縁ゲートを配設することにより、オン時に溝の側面のチャネルから半導体領域に電流が流入する点付近に発生する空乏領域を浅い拡散部分に対応するウエルの底面の凹所に閉じ込めて半導体領域内の電流流路の広がり角を増加させ、流路内の電流密度を減少させて絶縁ゲート制御半導体装置のオン電圧を低減できる。

【００３５】(c) 上述のような深い拡散部分がもつ耐圧の向上効果と，浅い拡散部分がもつオン電圧の低減効果は実施例で説明したように相互に干渉しないしは互いに減殺されることがないので、ウエルに深い拡散部分と浅

い拡散部分の双方を形成することにより、絶縁ゲート制御半導体装置の耐圧の向上とオン電圧の低減を同時に達成することができる。

【0036】(d) 溝ないしは絶縁ゲートを配列するピッチを縮小することにより電流容量を増加させるだけでなくオン電圧も低減できるので、絶縁ゲート制御半導体装置の微細パターン化を一層進めてその高周波特性を高めかつオン時の電流特性を向上させることができる。

また、本発明による絶縁ゲート制御半導体装置の製造方法では、ウエルを作り込むべき範囲の周縁部に深い拡散部分を所定深さにまず拡散した後、この範囲の表面に浅い拡散部分用の不純物を低いドーズ量で，周縁部の内側の表面の一部に不純物を所定ドーズ量でそれぞれイオン注入した上でそれらを同時熱拡散させることにより、深い拡散部分と浅い拡散部分と絶縁ゲート用部分を備えるウエルを少ない工程数でかつこれら各部分の深さをそれぞれ所望値に正確に管理しながら作り込むことができる。

【図面の簡単な説明】

【図１】本発明による絶縁ゲート制御半導体装置の一部拡大断面図である。

【図２】図１の絶縁ゲート制御半導体装置のオフ時とオン時の状態を示し、同図(a) はオフ時の等電位面の分布を，同図(b) はオン時の電流流路の分布をそれぞれ示す図１の要部拡大断面図である。

【図３】図１の絶縁ゲート制御半導体装置の耐圧特性を示す特性線図である。

【図４】図１の絶縁ゲート制御半導体装置のオン電圧特性を示す特性線図である。

【図５】図１の絶縁ゲート制御半導体装置に対する本発明の製造方法を主な工程ごとの状態で示し、同図(a) は深い拡散部分の拡散工程，同図(b) は浅い拡散部分用の不純物の導入工程，同図(c) はウエル用の不純物の導入工程，同図(d) は熱拡散工程，同図(e) は溝掘り込み工程，同図(f) は絶縁ゲート配設工程，同図(g) はソース層拡散工程，同図(h) は電極膜の配設工程の状態をそれぞれ示すウエハの要部拡大断面図である。

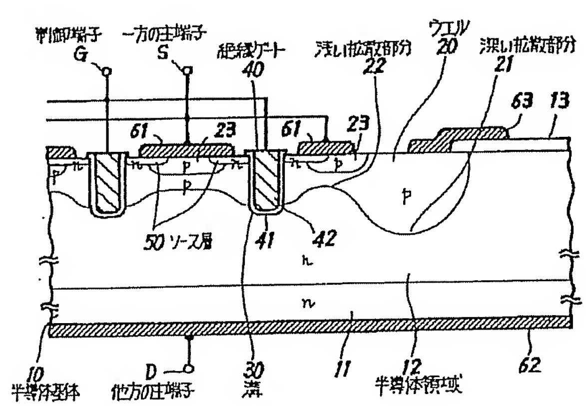
【図６】従来の絶縁ゲート制御半導体装置の一部拡大断面図である。

【図７】図６の絶縁ゲート制御半導体装置のオフ時とオン時の状態を示し、同図(a) はオフ時の等電位面の分布を，同図(b) はオン時の電流流路の分布をそれぞれ示す図６の要部拡大断面図である。

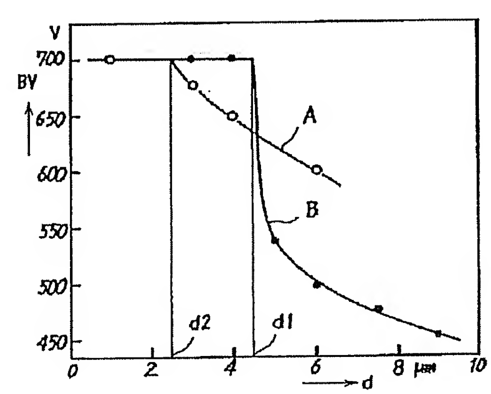
【符号の説明】

10	半導体基体ないしはウエハ
12	半導体領域ないしはエピタキシャル層
20	ウエル
21	ウエルの深い拡散部分
22	ウエルの浅い拡散部分
30	溝
40	絶縁ゲート
50	ソース層
A	本発明の絶縁ゲート制御半導体装置の耐圧特性
A1	本発明の絶縁ゲート制御半導体装置のオン電圧特性
A2	本発明の絶縁ゲート制御半導体装置のオン電圧特性
B	従来の絶縁ゲート制御半導体装置の耐圧とオン電圧特性
BV	絶縁ゲート制御半導体装置の耐圧
CP	オン時の電流流路
D	他方の主端子ないしはドレイン端子
d	溝の深さ
DZ	空乏領域
EP	オフ時の等電位面
FV	絶縁ゲート制御半導体装置のオン電圧
G	制御端子
p	溝の配列ピッチ
S	一方の主端子ないしはソース端子

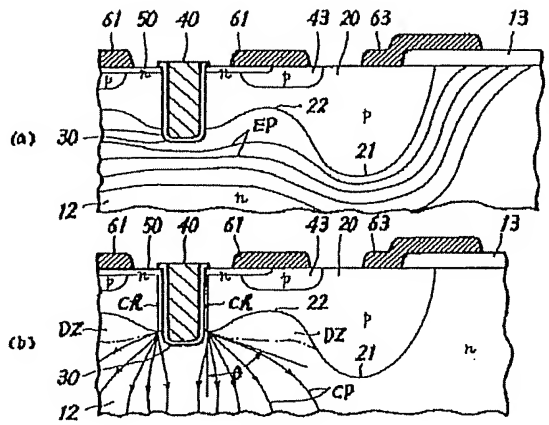
【図１】



【図３】

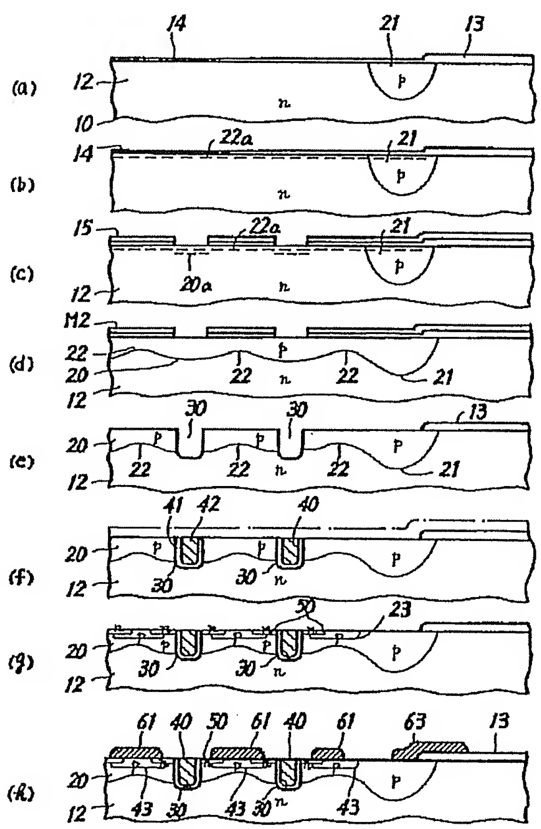


【図２】



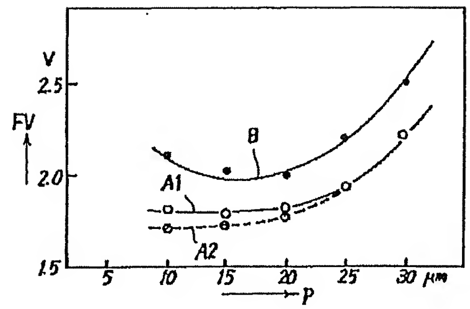
61 50 40 61 43 20 63 13
(a) 30 EP 22 p 21 n 12
(b) DZ 30 12 CR 22 DZ 21 CP θ p n

【図５】



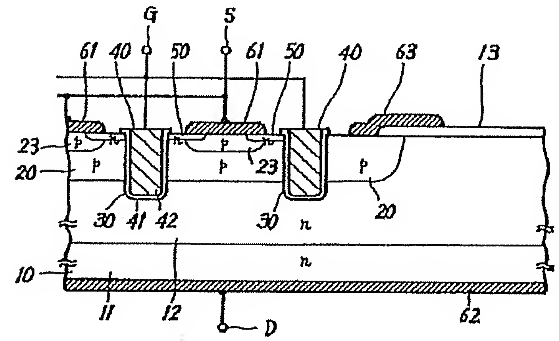
(a) 14 21 13 12 p n 10
(b) 14 22a 21 p n
(c) 15 22a 21 20a p n 12
(d) M2 22 20 12 p 22 n 22 21
(e) 30 30 13 20 p p 22 22 n 22 21 12
(f) 41 42 40 20 p p 30 30 n 12
(g) 50 23 20 30 30 n 12 p
(h) 61 40 50 61 40 61 63 13 20 12 43 30 43 30 n 43 p

【図４】



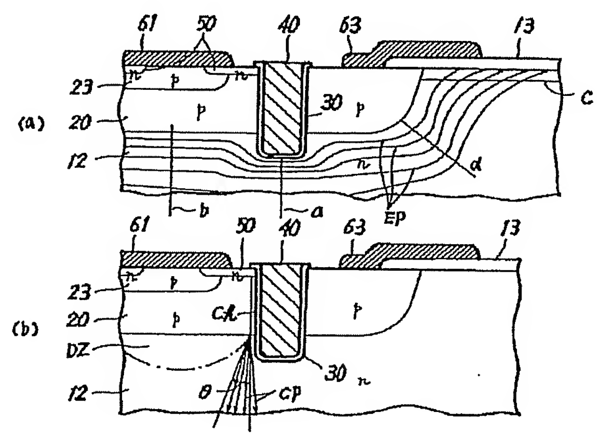
V
2.5
FV
2.0
1.5
B
A1
A2
5 10 15 20 25 30 μm
P

【図６】



G S
61 40 50 61 50 40 63 13
23 20 p p 23 p 20
30 41 42 30 n
10 n
11 12 D 62

【図７】



61 50 40 63 13
(a) 23 20 12 n p n p 30 p C d n EP a b
61 50 40 63 13
(b) 23 20 DZ 12 n p p CR θ CP 30 n